In the claims:

1. (currently amended) A method for processing a plurality of independent ~~instruction~~multi-packet thread threads comprising: retrieving a first ~~instruction~~multi-packet thread-packet from a first multi-packet thread ~~of instruction~~multi-packet thread~~s~~; retrieving a second ~~instruction~~multi-packet thread-packet from a second multi-packet thread ~~of instruction~~multi-packet thread~~s~~; ~~executing the first instruction~~multi-packet threadprocessing the first packet in a first stage of a processing pipeline; and forwarding the first ~~instruction~~multi-packet thread packet to a next stage of the processing while forwarding the second ~~instruction~~multi-packet thread packet to the first stage of the processing pipeline such that the first ~~instruction~~multi-packet thread and the second ~~instruction~~multi-packet thread-packets can be ~~executed~~ processed simultaneously in the processing pipeline, and wherein the independence of the ~~instruction~~multi-packet thread~~s~~multi-packet threads eliminates ~~pipeline~~ packet processing delays.

2. (currently amended) The method for processing the plurality of independent ~~instruction~~multi-packet thread-multi-packet threads according to claim 1, further comprising: transferring packet ~~data~~ from an input buffer to a packet task manager; dispatching the packet ~~data~~ from the packet task manager to an analysis machine; classifying the packet ~~data~~ in the analysis machine; and modifying and forwarding the packet ~~data~~ in a packet manipulator.

3. (currently amended) The method for processing the plurality of independent multi-packet~~instruction~~multi-packet thread threads according to claim 1, further comprising transferring the ~~data~~ packet after modifying and forwarding to an output buffer.

4. (Cancelled)

5. (currently amended) An apparatus for processing a plurality of independent multi-packet~~instruction~~multi-packet thread threads, said apparatus comprising: a processing pipeline including a plurality of stages coupled to receive and process the plurality of independent multi-packet~~instruction~~multi-packet thread threads such that, during a processing period, each of the plurality of stages of the processing pipeline is operating on a different one of the multi-

packet~~instruction~~multi-packet thread threads from the plurality of ~~instruction~~multi-packet thread threads, and wherein the independence of the ~~instruction~~multi-packet threads threads eliminates pipeline processing delays.

6. (original) The apparatus according to claim 5, further comprising; an analysis machine having multiple pipelines, wherein one pipeline is dedicated to directly manipulating individual data bits of a bit field; a packet task manager operationally connected to said analysis machine; and, a packet manipulator operationally connected to said analysis machine.

7. (original) The apparatus according to claim 6, wherein said analysis machine is multi-threaded.

8. (original) The apparatus according to claim 6, wherein said analysis machine has 32 threads.

9. (original) The apparatus according to claim 6, further comprising: a packet task manager operationally connected to said analysis machine; a packet manipulator operationally connected to said analysis machine; and a global access bus including a master request bus and a slave request bus separated from each other and pipelined.

10. (original) The apparatus according to claim 6, further comprising: an external memory engine operationally connected to said analysis machine; and a hash engine operationally connected to said analysis machine.

11. (previously presented) The apparatus according to claim 9, further comprising: packet input global access bus program code , stored in a computer readable memory and operable when executed to control a flow of data packet information from a flexible input data buffer to the analysis machine.

12. (previously presented) The apparatus according to claim 9, further comprising: packet data global access bus program code, stored in a computer readable memory and operable when

executed to control a flow of packet data between a flexible data input bus and the packet manipulator.

13. (previously presented) The apparatus according to claim 9, further comprising: statistics data global access bus software code used for connection of the analysis machine to the packet manipulator.

14. (previously presented) The apparatus according to claim 9, further comprising: private data global access bus software code used for connection of the analysis machine to an internal memory engine submodule.

15. (previously presented) The apparatus according to claim 9, further comprising: lookup global access bus software code used for connection of the analysis machine to an internal memory engine submodule.

16. (original) The apparatus according to claim 9, further comprising: results global access bus software code used for providing flexible access to an external memory.

17. (currently amended) The apparatus according to claim 5, wherein associated with each ~~instruction~~multi-packet thread is a thread identifier (TID) identifying a subset registers allocated to the corresponding independent ~~instruction~~multi-packet thread, the subset of registers selected from among a set of registers, and wherein the subsets associated with each one of the plurality of independent ~~instruction~~multi-packet threads are unique.

18. (original) The apparatus according to claim 9, further comprising: a bi-directional access port operationally connected to said analysis machine; an input buffer operationally connected to said analysis machine; and an output buffer operationally connected to said analysis machine.